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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,330	06/09/2006	William L. Keith	US030489US2	5371

24737 7590 01/25/2008

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
LE, TUNG X	

ART UNIT	PAPER NUMBER
2821	

MAIL DATE	DELIVERY MODE
01/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,330	KEITH ET AL.	
	Examiner	Art Unit	
	Tung X. Le	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/9/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' communication filed on June 09, 2006. In virtue of this filing, claims 1-18 are currently presented in the instant application.

Drawings

1. The drawings submitted on 06/09/2006 are accepted.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 6/9/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claims 3, 5, 8, 10, 12-14, and 16-17 are objected to because of the following informalities:

Claim 3, line 2, "a" should be changed to --the--;

Claim 5, line 2, "a" should be changed to --the--;

Claim 8, line 2, "a" should be changed to --the--;

Claim 10, line 2, "a" should be changed to --the--;

Claim 12, line 1, "10" should be change to –11--;

Claim 13, line 1, "10" should be change to –11--;

Claim 13, line 1, --the-- should be inserted before "filament";

Claim 14, line 1, "10" should be change to –11--;

Claim 16, line 1, "10" should be change to –11--; and

Claim 17, line 1, "10" should be change to –11--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (U.S. Publication No. 2002/0180380 A1).

With respect to claim 1, Lin discloses in figures 2-3 a method for open circuit voltage regulation for an electronic ballast comprising providing a regulating pulse width modulator (PWM) [22, 40] having an output voltage threshold limit [90]; sensing output voltage from the electronic ballast [C2, C3] to generate a sensed output voltage signal [66]; comparing the sensed output voltage signal to the output voltage threshold limit (having a comparator [28] for comparing the two signals); and limiting the output voltage when the sensed output voltage signal exceeds the output threshold limit [60] (paragraphs [0031, 0036]).

With respect to claim 2, Lin discloses in figures 2-3 that wherein the limiting the output voltage when the sensed output voltage signal exceeds the output voltage threshold limit comprises limiting pulse width from the regulating pulse width modulator [22].

With respect to claim 3, Lin discloses in figures 2-3 that the sensing output voltage from the electronic ballast to generate the sensed output voltage signal (the detecting circuit [60] having a sensed output voltage signal outputted to the generator [22]) comprises sensing tank current [42].

With respect to claim 4, Lin discloses in figures 2-3 that the sensing tank current comprises sensing voltage across a resistance capacitor [Rs, D5] and a common rail (a node between Rs and D5).

With respect to claim 5, Lin discloses that the sensing output voltage from the electronic ballast to generate the sensed output voltage signal comprises sensing output voltage directly (figures 2-3).

With respect to claim 6, Lin discloses in figures 2-3 a system for open circuit voltage regulation for an electronic ballast comprising means for modulating pulse width [22, 40] having an output voltage threshold limit [90]; means for sensing output voltage [C2, C3] fro the electronic ballast to generate a sensed output voltage signal [66]; means for comparing the sensed output voltage signal to the output voltage threshold limit (having a comparator [28] for comparing the two signals); and means for limiting the output voltage when the sensed output voltage signal exceeds the output voltage threshold limit [60] (paragraphs [0031, 0036, 0042]).

With respect to claim 7, Lin discloses in figures 2-3 that wherein the means for limiting the output voltage when the sensed output voltage signal exceeds the output voltage threshold limit comprises means for limiting pulse width from the regulating pulse width modulator means [22].

With respect to claim 8, Lin discloses in figures 2-3 that the means for sensing output voltage from the electronic ballast to generate the sensed output voltage signal (the detecting circuit [60] having a sensed output voltage signal outputted to the generator [22]) comprises means for sensing tank current [42].

With respect to claim 9, Lin discloses in figures 2-3 that the means for sensing tank current comprises means for sensing voltage across a resistance capacitor [Rs, D5] and a common rail (a node between Rs and D5).

With respect to claim 10, Lin discloses that the means for sensing output voltage from the electronic ballast to generate the sensed output voltage signal comprises means for sensing output voltage directly (figures 2-3).

With respect to claim 11, Lin discloses in figures 2-3 an open circuit voltage regulation circuit for an electronic ballast comprising an filament current sensing circuit [60] operably connected to an output of the electronic ballast and generating a sensed output voltage signal [66]; and a regulating pulse width modulator [22] receiving the sensed output voltage signal and operably connected to control voltage at the output threshold limit [90]; wherein the regulating pulse width modulator limits the voltage at the output of the electronic ballast when the sensed output voltage signal exceeds the output voltage threshold limit [60] (paragraphs [0031, 0036, 0042]).

With respect to claim 12, Lin discloses that the regulating pulse width modulator limits the voltage at the output of the electronic ballast by limiting pulse width (figure 2 and para [0042]).

With respect to claim 13, Lin discloses in figures 2-3 that wherein the filament current sensing circuit is responsive to tank current [Rs, D5].

With respect to claim 14, Lin discloses in figures 2-3 that the ballast further comprises a tank circuit [Rs, D5] operably connected to the output of the electronic ballast and having a resonant capacitor [D5]; and the filament current sensing circuit comprises a resistance [Rs] between the resonant capacitor and a common rail (figure 2).

With respect to claim 15, Lin discloses in figures 2-3 that the regulating pulse width modulator has a set trip level (the threshold level of the signal [66]) for the output voltage threshold limit and the resistance is sized (figure 2) so that the sensed output voltage signal exceeds the set trip level when the electronic ballast has an open circuit (paragraph [0035]).

With respect to claim 16, Lin discloses in figures 2-3 that the circuit further comprises a high voltage driver [50] operably connected to be driven by the regulating pulse width modulator [22], and the regulating pulse width modulator limits the voltage at the output of the electronic ballast by driving the high voltage driver at a limited pulse width (paragraphs [0031, 0036, 0042]).

With respect to claim 17, Lin discloses in figures 2-3 that the ballast further comprises a tank circuit [Rs, D5] operably connected to the output of the electronic ballast and having a resonant capacitor [D5]; and the filament current sensing circuit comprises a resistance [Rs] between the resonant capacitor and a common rail (figure 2).

With respect to claim 18, Lin discloses that the filament current sensing circuit is selected from the group consisting of a resistive voltage divider (having a sensing voltage divider [C2-C3] in figure 2).

Citation of Relevant Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Stevanovic et al. (U.S. Patent No. 5,910,709) discloses a florescent lamp ballast control for zero voltage switching operation over wide input voltage protection.

Prior art Fujimura et al. (U.S. Patent No. 6,239,558 B1) discloses a system for driving a cold cathode fluorescent lamp connected to a piezoelectronic transformer.

Prior art Crouse et al. (U.S. Publication No. 2006/0175983 A1) discloses a software controlled electronic dimming ballast.

Inquiry

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Le whose telephone number is 571-272-6010. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Owens can be reached on 571-272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Tung Le
AU 2821

January 21, 2008

THUY V. TRAN
PRIMARY EXAMINER